

Features

CPU

- ✓ High-performance 8051-compatible 8-bit CPU
 - 1 instruction = 1~3 machine cycle(s)
 - 1 machine cycle = 4 clock cycles (typical)
- ✓ CPU operating clock can be configured:
 - Internal clock :7.5 MHz/15 MHz/30 MHz(nominal)
 - External clock: Contact smart card input CLK supply via C3 (ISO/IEC 7816)

Memories

- FLASH
 - ✓ Size:132 KB
 - ✓ Page size:512 bytes
 - ✓ Erase and program operation: Page Erase and Byte Program
 - ✓ Typical time: erasing 4ms, programming 25µs
 - ✓ Bit logic: 1b after erasing, 0b after programming to be 0b
 - ✓ Usage: code and data
 - Program can surmount the 64 KB limit, using CODE Banking
 - High 56 KB FLASH is accessible from XDATA
- RAM
 - ✓ Size: 2.25 KB
 - 2048 bytes in XDATA
 - 256 bytes in IDATA
- OTP
 - ✓ User OTP:224bytes
 - ✓ SN:17 bytes

Algorithms and Peripherals

- Symmetric algorithms
 - ✓ DES/T-DES
- Peripherals
 - ✓ CRC: 16-bit CRC-CCITT
 - ✓ TRNG: True Random Number Generator, for secure transactions
 - ✓ Timer: One 16-bit timer, one ETU timer

Interfaces

- ISO/IEC 7816-3 serial interface
 - ✓ UART supporting ISO/IEC 7816-3 T=0/T=1 protocol and 10 baud rates:
F/D = 11H, 12H, 13H, 18H, 91H, 92H, 93H, 94H, 95H,96H
 - ✓ Support GSM power consumption standards, including Clock Stop mode



THC20F17BD-V20

**Contact Smart
Card IC**

132 KB FLASH

2.25 KB RAM

Beta

**Security**

- ✓ Scrambling data storage
- ✓ High/low voltage and high/low clock frequency detectors
- ✓ CLK filter(ISO/IEC 7816 external clock)
- ✓ Glitch detection
- ✓ Security Certification: EAL4+

Work parameters (Note1)

Symbol	Name	Conditions	Min	Typical	Max	Unit
TDES	Time for Executing 64-bit DES Encryption		17		17	clock cycle
TPE	Time for Erasing a Page		2	4	4	ms
TBP	Time for Program a Byte			25		us
TDR	Data Retention			10		year
NPE	Page Endurance			100K		Cycle
f _{EXT}	External Clock Freq.		1		5	MHz
f _{INT}	Internal Clock. Freq.		7.5		30	MHz
V _{CC}	Supply Voltage		1.62		5.5	V
I _{CC}	Supply Current	V _{CC} = 5.0V			10	mA
		V _{CC} = 3.0V			6	mA
		V _{CC} = 1.8V			4	mA
I _{SB}	Standby Current (Clock Stop)	V _{CC} = 5.0V			200	μA
		V _{CC} = 3.0V			100	μA
		V _{CC} =1.8V			100	μA
T _{AMB}	Ambient Temperature		-40		85	°C
V _{ESD}	ESD Protection	HBM	4			kV

Note1: This document is a preliminary version, data and descriptions (including this table) can not be a formal evidence for performance and functions of the IC.

Descriptions

THC20F17BD-V20 is an 8-bit CPU contact smart card IC with a total of 132 KB FLASH and hardware DES/TRNG/CRC, suitable for general IC card applications, such as SIM, Banking Card, CA in Paid TV, Campus Card, City Card, etc.

COS developers can flexibly partition the 132 KB FLASH to store code and data.

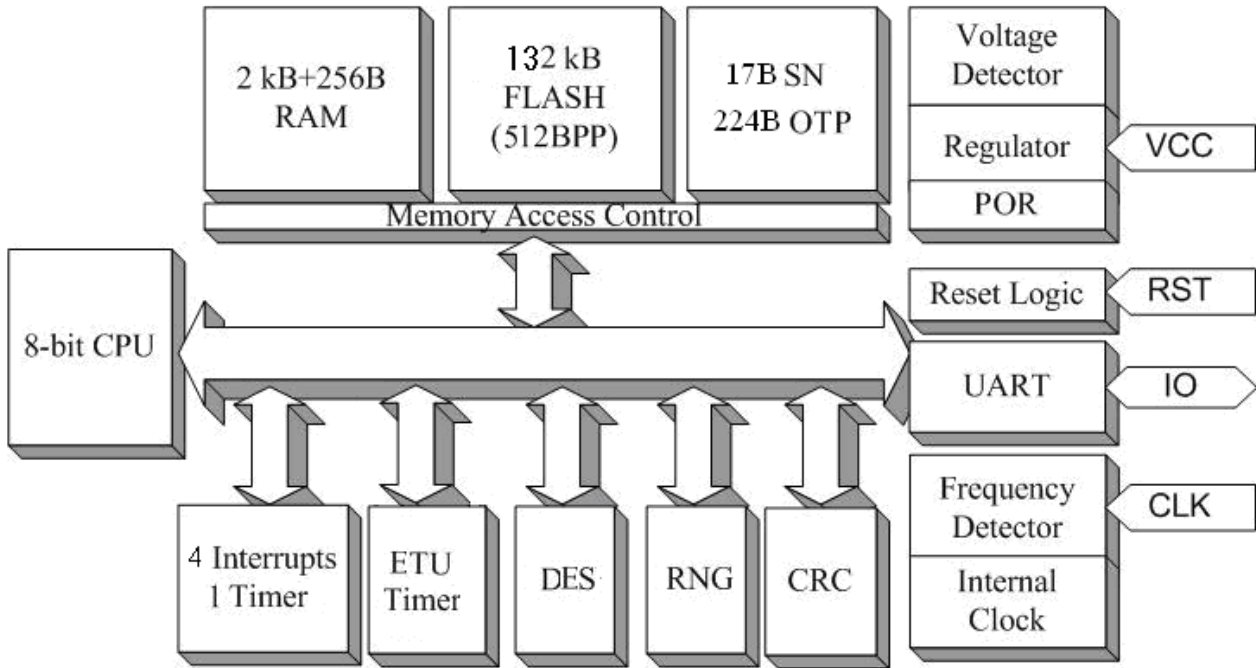
COS can access the high 56 KB FLASH area (meet the requirements of the 32 KB SIM application) from XDATA.

COS can access all FLASH area from CODE, because the 64 KB limit can be surmounted by CODE banking.

To facilitate software development, the IC embeds hardware DES/ TRNG/ CRC. COS developers can enjoy smaller code size and less execution time.

For better security and reliability, the IC offers many hardware security features, e.g., Write-protection for a configurable FLASH area, High/low voltage and high/low clock frequency detection, etc.

Structure



Development Toolkits

- ✓ SCDS series Hardware Emulator(Target board inside)
- ✓ IDE:Keil uVision2/3/4
- ✓ Demo project and API(Application Program Interface)codes
- ✓ User Manual and Application Notes
- ✓ The UDVG software tool to generate COS downloading script with user desired format

Package and Pin Definitions

Different packages are available, e.g., wafer / module / card, etc.

Listed are pin definitions for a card package.

Signal Name	Function Descriptions	Contact defined in ISO/IEC 7816-2
VCC	Power Supply Voltage	C1
GND	Ground	C5
CLK	Clock Input	C3
RST	Reset Signal	C2
I/O	Data Input/Output	C7
NC	Not Connected	C4, C6, C8



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