Features

CPU

- ✓ High-performance 32-bit ARM core
- ✓ 3-stage pipeline
- ✓ Little Endian
- ✓ CPU clock could be configured
  - internal clock :3.5/7/9/14/28MHz configurable
  - External clock: Contact smart card input CLK supply via C3 (ISO/IEC 7816)

➢

Memory

- ➢ ROM
  - ✓ Size:8 KB
  - ✓ Usage: For storage of bootloader only
- ➢ FLASH
  - ✓ Size:548 KB
  - ✓ Page size:256/512 Bytes
  - ✓ Erase and program operation: page erasing, page programming
    - Page Erase is mandatory before a Page Program operation (consecutive Page Program is NOT supported)
- ➢ Typical time: erasing 3ms, programming 2 ms
  - ✓ Bit logic: 1b after erasing, 0b after programming to be 0b
  - ✓ Usage: data and code
- ➢ RAM
  - ✓ Size:18 KB
    - 2KB crypto RAM included
  - ✓ Usage: data and code
- ➢ OTP
  - ✓ User OTP:112 Bytes
  - ✓ SN:8 Bytes
- ➢
- ➢ **Algorithms and Peripherals**
- ➢ Symmetric algorithms
  - ✓ DES/T-DES
- ➢ Asymmetric algorithms
  - ✓ RSA
- ➢ Peripherals
  - ✓ CRC:16-bit CRC-CCITT
  - ✓ TRNG: True Random Number Generator, for secure transactions
  - ✓ TIMER: Three 16-bit Timers, one ETU timer
  - ✓ WUT:Wake-up timer

Interface

- ➢ ISO/IEC 7816-3 serial interface

THC80F09BC

32-BIT Contact Smart Card IC

548 KB FLASH

18 KB RAM

8 KB ROM

Beta

- ✓ Slave(ICC) and/or master(IFD)
- ✓ UART supporting ISO/IEC 7816-3 T=0/T=1 protocol and 10 baud rates: F/D = 11H, 12H, 13H, 18H, 91H, 92H, 93H, 94H, 95H,96H,
- ✓ Interface DMA supported
- ✓ Dedicated ETU Counter for procedure byte (60H) generation
- ✓ Support GSM power consumption standards, including Clock Stop mode

➢ Serial peripheral interface(SPI)
- ✓ Hardware SPI master controller
- ✓ Max speed: 14 Mbps

➢ SWP
- ✓ Compliant with ETSI TS 102 613
- ✓ DMA

➢ GPIO
- ✓ 48 GPIOs
- ✓ 2 GPIOs can wake up chip via interrupt
- ✓ 2 GPIOs multiplexed with ISO7816 Master
- ✓ 3 GPIOs multiplexed with SPI
- ✓ 6 GPIOs multiplexed with JTAG
- ✓ 1 GPIO multiplexed with ISO7816 Slave SIO

Security
- ✓ WDT(Watch Dog Timer)
- ✓ Bus scrambling, encrypted data storage
- ✓ High and low voltage detectors
- ✓ High and low clock frequency detectors
- ✓ Clock filter(ISO/IEC 7816 external clock)
- ✓ Security Certification: EAL4+
- ✓ Anti-DPA

Operating Characteristics (Note 1)

Symbol	Name	Conditions	Min	Typical	Max	Unit
T_{DES}	Time for DES encryption or decryption			17		clock
T_{SE}	Time for Erasing a Page			3		ms
T_{SP}	Time for Programming a Page			2		ms
T_{DR}	Flash Data Retention		10			year
N_{SE}	Flash Endurance		100 k			Cycle
f_{EXT}	External Clock Freq.		1		5	MHz
f_{INT}	Internal Clock. Freq.		3.5		28	MHz
V_{CC}	Supply Voltage		1.62		5.5	V
I_{CC}	Supply Current	VCC= 5.0V			10	mA
		VCC= 3.0V			6（Note 2）	mA
		VCC= 1.8V			4（Note 3）	mA

I_{SB}	Standby Current (Clock Stop)	VCC= 5.0V			200	μA
		VCC= 3.0V			100	μA
		VCC= 1.8V			100	μA
T_{AMB}	Ambient Temperature		-40		85	°C
V_{ESD}	ESD Protection	HBM	4			kV

Note 1: This document is a preliminary version, data and descriptions (including this table) can not be a formal evidence for performance and functions of the IC.
Note 2: When operating at external clock or 14MHz (or lower) internal clock.
Note 3: When operating at external clock or 9MHz (or lower) internal clock.

Descriptions

THC80F09BC is designed for general IC card applications, such as SIM (native or JAVA), Banking Card, CA in Pay-TV, Campus Card, City Card, etc.

THC80F09BC is based on a high performance, high security, low power consumption, 32-bit embedded RISC CPU core. It has Von Neumann architecture, with a single 32-bit data bus carrying both instructions and data. THC80F09BC has two kinds of physical memory:

- 548 KB FLASH for both program and data storage.
- 18 KB RAM for both program and data storage.

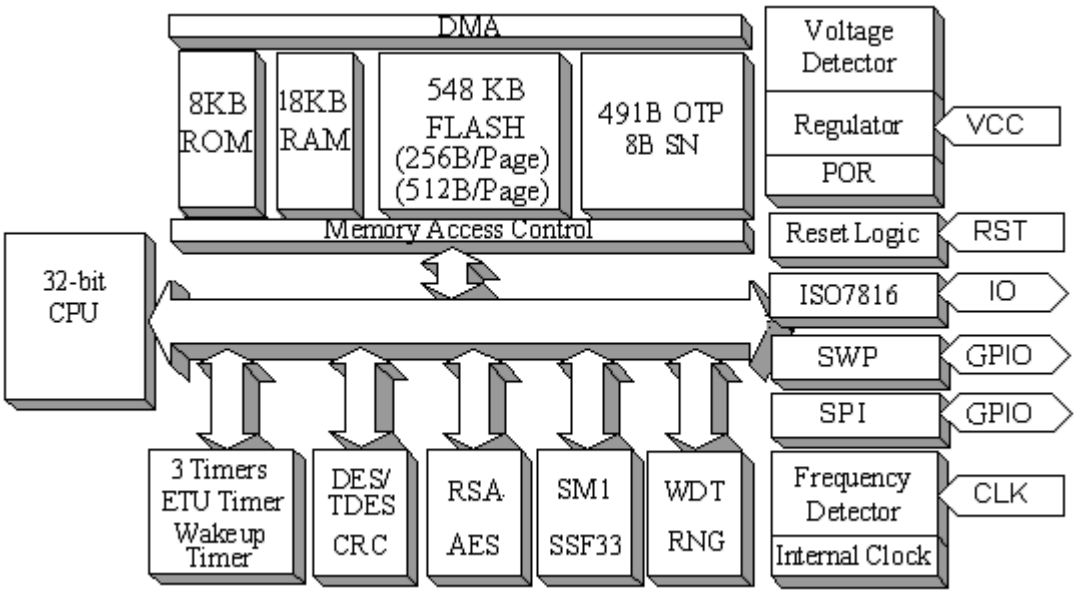
The internal 548 KB FLASH memory can be used as program and data memory. That is, COS can be downloaded in and executed from the FLASH memory. In addition, the remained region of FLASH memory can be used for data storage.

- Both erase and program operation are performed in 256-byte /512-byte page unit
- Byte Erase and Byte Program operation can NOT be supported
- A Page should always be erased before it can be programmed. In other words, consecutive programming is NOT supported
- For a general FLASH modification flow, it is recommended to be “Page Read -> modify buffer -> Page Erase -> Page Program”

To facilitate software development, the IC embeds hardware DES, TRNG, CRC, etc. COS developers can enjoy smaller code size and less execution time.

For better security and reliability, the IC offers many hardware security features, e.g., High/low voltage and high/low clock frequency detection, etc.

Structure



Development Toolkits

- AK100 Emulator
- TMC Target board
- IDE:Keil uVision3/4
- Demo project and API(Application Program Interface)codes
- User Manual and Application Notes
- The UDVG software tool to generate COS downloading script with user desired format

Package and Pin Definitions

The chip could be shipped in the types of package such as wafer, module and card.
Listed are pin definitions for a card package.

Signal Name	Function Descriptions	Contact defined in ISO/IEC 7816-2
VCC	Power Supply Voltage	C1
GND	Ground	C5
CLK	Clock Input	C3
RST	Reset Signal	C2
I/O	Data Input/Output	C7
SWP	SWIO contact	C6
NC	Not Connected	C4, C8

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