Features

CPU

- ✓ High-performance/Low Power 32-bit ARM core
- ✓ 3-stage pipeline
- ✓ Little-endian
- ✓ System clock frequency can be configured
  - Internal clock: 4MHz, 8MHz, 10.56MHz, 16MHz
  - External clock: contact interface clock and contactless interface clock

Memory

- ➢ ROM
  - ✓ Size: 64 KB（56 KB, user program area）
- ➢ EEPROM
  - ✓ Size: 32 KB
  - ✓ Page size: 64 Bytes
  - ✓ Sector size: 4 KB
  - ✓ Erase and program operation: sector/page/byte erase, page/byte program
  - ✓ Typical time: erase 2.3ms, program 2.3ms
  - ✓ Bit logic: 0b after erasing, 1b after programming 1b
  - ✓ Usage: data and code
- ➢ FLASH
  - ✓ Size: 400 KB
  - ✓ Page size: 256 Bytes
  - ✓ Erase and program operation: page erase page program
    - Page Erase is mandatory before a Page Program operation (consecutive Page Program is NOT supported)
  - ✓ Typical time: erase 3.0ms, program 2.0ms
  - ✓ Bit logic: 0b after erasing, 1b after programming 1b
  - ✓ Usage: data and code
- ➢ RAM
  - ✓ Size: 14.25 KB
    - 10 KB, CPU data area
    - 4 KB, CCP data area, CPU accessible
    - 0.25 KB, RF buffer
- ➢ OTP
  - ✓ 16 Bytes SN
  - ✓ 10 Bytes UID

Algorithms and Peripherals

- ➢ Symmetric algorithms
  - ✓ DES/T-DES
  - ✓ SM1
  - ✓ SSF33
- ➢ Asymmetric algorithms

THD86EF59AC 32-bit Dual Interface Smart Card IC

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400 KB FLASH

64 KB ROM

32 KB EEPROM

14.25 KB RAM

Beta

- ✓ RSA (CCP, Max 2048 bits)
- ✓ ECC (CCP)
- ✓ SM2 (CCP)
- ➢ Hash algorithm
  - ✓ SHA1 (CCP)
  - ✓ SM3 (CCP)
- ➢ Peripherals
  - ✓ CRC: 16-bit CRC-CCITT
  - ✓ TRNG: True Random Number Generator, for secure transactions
  - ✓ CCP: Cryptographic Coprocessor
  - ✓ DMA: Data block copy or comparison
  - ✓ Timer: SYSTICK and TIMER0 timers

Interfaces

- ➢ ISO/IEC 7816 Master/Slave interface
  - ✓ Support T=0/T=1 protocol
  - ✓ Support 9 baud rates: F/D = F/D = 11H, 12H, 13H, 18H, 91H, 92H, 93H, 94H, 95H
  - ✓ 3BH and 60H are sent automatically by hardware
  - ✓ Support GSM power consumption standards
  - ✓ Support FIFO mode, 5 bytes
  - ✓ Contactless interface and contact interface (T=0) can work simultaneously
  - ✓ When contactless transaction is in progress, contact interface can automatically cache the contact command header and send the NULL byte 60H
- ➢ ISO/IEC 14443 interface
  - ✓ Compatible with ISO/IEC 14443 Type A and Type B
  - ✓ Type Aand Type B auto-adaption
  - ✓ Support baud rates:
    - Normal rate: 106 kbit/s
    - Enhanced rates: 212 kbit/s, 424 kbit/s
  - ✓ TR1, SOF, EOF, EGT in Type B response frame can be configured by software
  - ✓ Support Crypto1
- ➢ GPIO
  - ✓ 4 pins
  - ✓ Multiplex with ISO7816Master interface
- ➢ SPI
  - ✓ Support Master and Slave modes
  - ✓ Max speed: 5 Mbps

Security

- ➢ Environment monitor circuit
  - ✓ High/Low Voltage detection
  - ✓ High/Low Frequency detection
  - ✓ High/Low Temperature detection
  - ✓ Power Glitch Sensor (GS)
  - ✓ Light sensor

➢ ANTI-SPA and ANTI-DPA ATTACK
➢ Watchdog circuit
➢ Memory storage encryption
➢ Bus encryption
➢ EAL4+ security certification

Work parameters

Symbol	Parameter		Minimum	Typical value	Maximum	Unit
T_{PE}	Flash page erasing time			3.0		ms
T_{PP}	Flash page programming time			2.0		ms
T_{EE}	EEPROM byte/page/sector erasing time			2.3		ms
T_{EP}	EEPROM byte/page programming time			2.3		ms
T_{DR}	Flash/EEPROM data retention		10			year
N_{PE}	Flash/EEPROM page endurance		100k			cycle
V_{CC}	Supply Voltage		1.55		6	V
V_{IO}	IO Voltage		1.55		6	V
V_{ESD}	ESD protection (HBM)				4.0	kV
T_{OPR}	Working temperature		-40		85	℃
I_{SB}	Standby Current (Clock Stop)	V_{CC}= 5.0V			200	μA
		V_{CC}= 3.0V			100	μA
		V_{CC}=1.8V			100	μA
f_{EXT}	Contact interface external clock freq.		1		5	MHz
f_{INT}	Internal clock freq.		4		16	MHz
f_{CCP}	CCP clock freq.		4		32	MHz
T_{KGrsa}	RSA key generation (2048 bits)				13	s
T_{KGsm2}	SM2 key generation (256 bits)				41.3	ms

Note: This document is a Beta version, data and descriptions (including this table) cannot be a formal evidence for performance and functions of the IC.

Descriptions

THD86EF59AC is a 32 bits CPU dual interface smart card IC with ROM，FLASH，EEPROM and RAM memory, hardware DES / TRNG / CRC / SM1 / SSF33 and Cryptographic Coprocessor (CCP). It is suitable for contactless /contact smart card applications, such as payment card, ID card, bank card, etc.

Compatible with ISO/IEC14443 part 1/2/3 Type A and Type B protocol, the card can be operated by a standard Type A or Type B reader at a distance up to 10 cm. Software can configure the card to be automatically adaptable to Type A and Type B protocol, or to be only Type A or Type B.

It is also compatible with ISO/IEC 7816 part 1/2/3 T=0 and T=1 protocol. The contactless interface and the contact interface (ISO/IEC 7816 T=0) can work simultaneously. The 7816 command header can be received automatically and the NULL byte 60H can be transmitted automatically, while contactless interface is busy in contactless transaction.

For software development convenience, the IC provides hardware DES/ TRNG/ CRC/SM1/SSF33 and CCP to efficiently cut software code size and to save transaction time. The IC support DMA to copy data by hardware to accelerate data copy, data comparison, FLASH reading and writing, and cryptographic algorithms.

For better security and reliability, the IC provides enhanced security features, e.g., Electrical Environment Detectors, and Anti-SPA/DPA protections.

Chip Structure
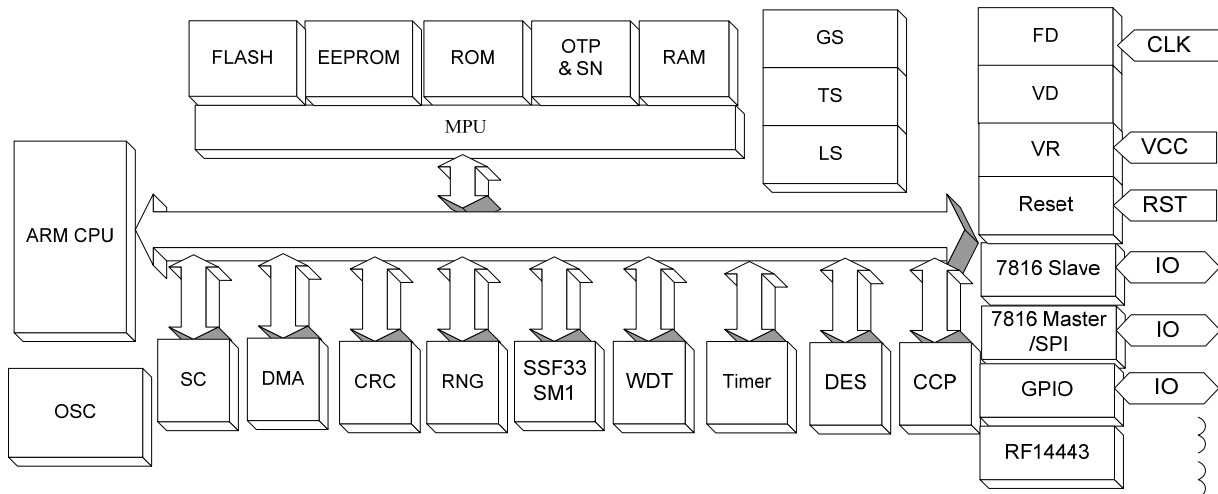
Development Toolkits

- ✓ ULINK2 Emulator
- ✓ TMC target board
- ✓ IDE：Keil uVision4
- ✓ Demo project and API (Application Program Interface) codes
- ✓ User Manual and Application Notes
- ✓ The UDVG software tool to generate COS downloading script with customized format

Package and Pin Definitions

Package:

Package	Remark	Application
Wafer	8-inch	Any
Module	Contact/contactless/ dual-interface	Smart card
Card	Contact/contactless/ dual-interface	Smart card
QFN32	-	
DIP40	-	

Pin Definitions:

Number	Name	Description
1	VA	Contactless card antenna interface

2	VB	Contactless card antenna interface
3	P0.0/S7816CLK	GPIO P0.0 or contact card (ISO7816 slave) interface clock signal
4	P0.1/S7816_RST	GPIO P0.1 or contact card (ISO7816 slave) interface reset signal
5	P0.2/S7816_SIO	GPIO P0.2 or contact card (ISO7816 slave) interface data signal
6	P1.0/SPI_MISO/M7816_CLK	GPIO P1.0 or SPI MISO signal or ISO7816 master interface clock signal
7	P1.1/SPI_CLK/M7816_RST	GPIO P1.1 or SPI clock signal or ISO7816 master interface reset signal
8	P1.2/SPI_MOSI/M7816_SIO	GPIO P1.2 or SPI MOSI signal or ISO7816 master interface data signal
9	P1.3/SPI_SS_N	GPIO P1.3 or SPI CS signal
10	VCC	Power
11	GND	GND

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